REMARKS

In the Office Action the Examiner rejected all claims 1-10 and 12-17 under examination under 35 U.S.C. 103 for being obvious. Claims 4-10 and 12-17 remain in the application.

The rejection for obviousness was based on Matsumoto and Rutten. Matsumoto teaches a substrate contact that is performed after formation of the transistor. Thus, the anneal that is performed on the doped region 11, which is the contact region, will also be experienced by the source/drains 8 as shown in FIG. 1A of Matsumoto. This is contrasted with applicant's invention at page 9, lines 1-8. Further, the implant to form region 11 results in the need for an extra masking step for Matsumoto. The contact mask for the P channel transistors can be the same for both the implant of region 11 and for the source/drain contacts because the P channel source drains are of the same conductivity type as contact 11. The N channel source/drains, however, would be degraded by this implant to form contact region 11. Thus, in Matsumoto the N channel transistors should have a different mask for the source/drain contacts than for the mask that is for implanting region 11 and the P channel source/drains.

Rutten is addressing a different issue than that confronted by Matsumoto and applicant. Rutten is forming a region that forms a PN junction. FIGs. 1-4, for example, show a P+ region 50 formed within an N region 9. The substrate 1 is P+ so that the contact region 50 is separated from the substrate 1 by region 9 of opposite conductivity type. This region 50 thus does not serve as contact region to either region 9 in the substrate or substrate 1.

Claim 4 has been amended to independent form and clarifies that the contact is a substrate contact and further clarifies the timing of certain aspects of the claimed method. Independent claims 10 and 17 also have been clarified in this regard. The timing of the implant, prior to the transistor formation, is beneficial as pointed out above compared to the timing described by Matsumoto. The claimed timing results in the benefit of being able to form the contact region, region 26 for example, with the same mask that is used to form isolation region 30. Accordingly, applicant submits that the two references are not obvious to combine in order to achieve the claimed method.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicant believes the application is in condition for allowance which action is respectfully solicited. Please contact the below-signed if there are any issues regarding this communication or otherwise concerning this application.

Respectfully submitted,

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CLAIMS - VERSION WITH MARKINGS TO SHOW CHANGES MADE

4. (Amended) [The] A method [of claim 2, wherein] for forming [the transistor further comprises] a contact to a semiconductor substrate of a first conductivity type, comprising:

providing a semiconductor stack including an active layer formed on a first insulator layer, wherein the first insulator layer is formed on the semiconductor substrate;

implanting the semiconductor substrate through the first insulator layer with a first species to form a first doped region within the semiconductor substrate, wherein the first doped region is the first conductivity type and is more heavily doped than the semiconductor substrate;

after the implanting, forming a gate dielectric on the active layer;

forming a gate electrode on the gate dielectric; [and]

forming a source region in the active layer adjacent a first side of the gate electrode; [and]

forming a drain region in the active layer adjacent a second side of the gate electrode, wherein the second side is opposite the first side; and

forming a first contact electrically connected to the first doped region

[and further comprising:

implanting after etching the portion of the active layer and before forming the gate electrode].

10. (Amended) A method of forming a contact to a semiconductor substrate of a first conductivity type, comprising:

providing a semiconductor stack including an active layer formed on a first insulator layer, wherein the first insulator layer is formed on [a] the semiconductor substrate;

forming a gate dielectric over the active layer;

forming a gate electrode over the gate dielectric;

forming source and drain regions in the active layer and adjacent the gate electrode as to form a channel region underneath the gate electrode;

removing a portion of the active layer;

forming a second insulator layer adjacent the active layer and on the first insulator layer;

forming a doped region within the substrate before forming the gate electrode, wherein the doped region is the first conductivity type and is more heavily doped than the semiconductor substrate;

forming a first opening in the second insulator layer and the first insulator layer; and

forming a conductive material within the first opening.

17. (Amended) A method of forming a contact to a semiconductor substrate of a first conductivity type, comprising:

providing a semiconductor stack including an active layer formed on a first insulator layer, wherein the first insulator layer is formed on [a] the semiconductor substrate;

removing a portion of the active layer;

forming a second insulator layer adjacent the active layer and on the first insulator layer;

forming an opening in the second insulator layer and the first insulator layer;

forming a conductive material within the opening; [and]

forming a doped region within the semiconductor substrate under the area of the opening before forming [a] the conductive material within the opening, wherein the doped region is the first conductivity type and is more heavily doped than the substrate; and

forming a transistor in the active layer after forming the doped region.